

Docket No.: 60188-044



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SP  
2-10-04  
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277  
Hirokazu YONEZAWA, et al. : Confirmation Number:  
Serial No.: 09/810,518 : Group Art Unit: 2123  
Filed: March 19, 2001 : Examiner:

For: APPARATUS AND METHOD FOR CALCULATING TEMPORAL  
DETERIORATION MARGIN AMOUNT OF LSI, AND LSI INSPECTION METHOD

INFORMATION DISCLOSURE STATEMENT

Mail Stop Information Disclosure  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

RECEIVED

FEB 09 2004

Technology Center 2100

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

Each non-English language reference was first cited in a corresponding foreign application search report or office action and its relevance discussed therein. A copy of the

09/810,518

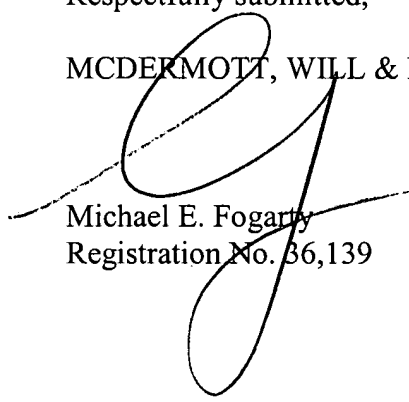
foreign search report or office action, together with an English language version thereof, is attached for the Examiner's information.

The reference JP 10-124565A was previously submitted in the Information Disclosure Statement filed on March 19, 2001.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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**Date: February 6, 2004**



SHEET 1 OF 1

INFORMATION DISCLOSURE  
CITATION IN AN  
APPLICATION

(PTO-1449)

ATTY. DOCKET NO.  
**60188-044**SERIAL NO.  
**09/810,518**APPLICANT  
**Hirokazu YONEZAWA, et al.**FILING DATE  
**March 19, 2001**GROUP  
**2123**

## U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US			
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## FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes - Number - Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
						Yes	No
		JP 11-219380 A (w/ English Abstract)	08/10/1999	MATSUSHITA ELECTRIC IND. CO., LTD.			

## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		Y. KAWAKAMI et al., "Gate-Level Aged Timing Simulation Methodology for Hot-Carrier Reliability Assurance", Proc. ASP-DAC 2000, IEEE, January 28, 2000, pages 289-294.

EXAMINER

DATE CONSIDERED

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.